

Features

- Modular and scalable ASiS™ (Application Specific Integrated System) architecture in CMOS technology
- Ideally suited for embedded portable applications
- 12 channel parallel receiver with programmable Zoom Correlators™
- Fast signal acquisition with dedicated QwikLock™ search engine
- Integrated low-power 16-bit proprietary VS DSP-core
- On-chip SRAM memories
- 3V power supply
- Low power consumption enabled by PowerMiser™
- Small Form Factor – 144-pin BGA
- Interface to an external RF front-end
- Input master clock frequency doubler

Description

The *uN8031B* is a highly integrated GPS receiver for embedded portable solutions. It obsoletes the earlier *uN8031A* and includes all baseband functions needed for GPS signal acquisition, tracking and navigation. Two asynchronous serial interfaces provide for navigation solution output and differential correction data input. A programmable general purpose I/O interface is also included. External non-volatile memory can be connected using an external bus interface. A dedicated high-performance search engine using patented QwikLock™ architecture enables a rapid search of available satellites. An advanced tracking unit employing Zoom Correlators™ insures that positioning is possible even in severe conditions like in urban canyons and under foliage. A complete GPS receiver built with a *uN8031B* baseband and a *uN8021B* RF front-end needs only a handful of external components, keeping the overall bill of materials to a minimum as illustrated below.

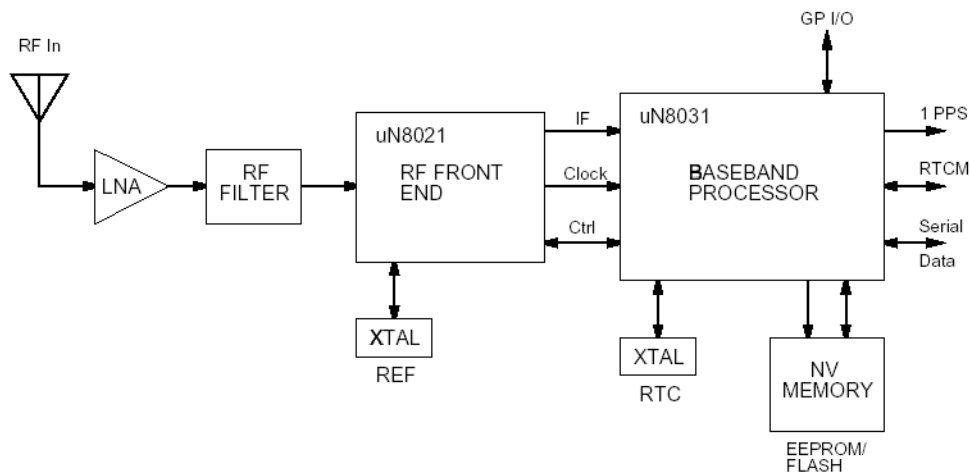


Figure 1. GPS Receiver Based on u-Nav Chip Set

Block Diagram

The uN8031B block diagram is shown below:

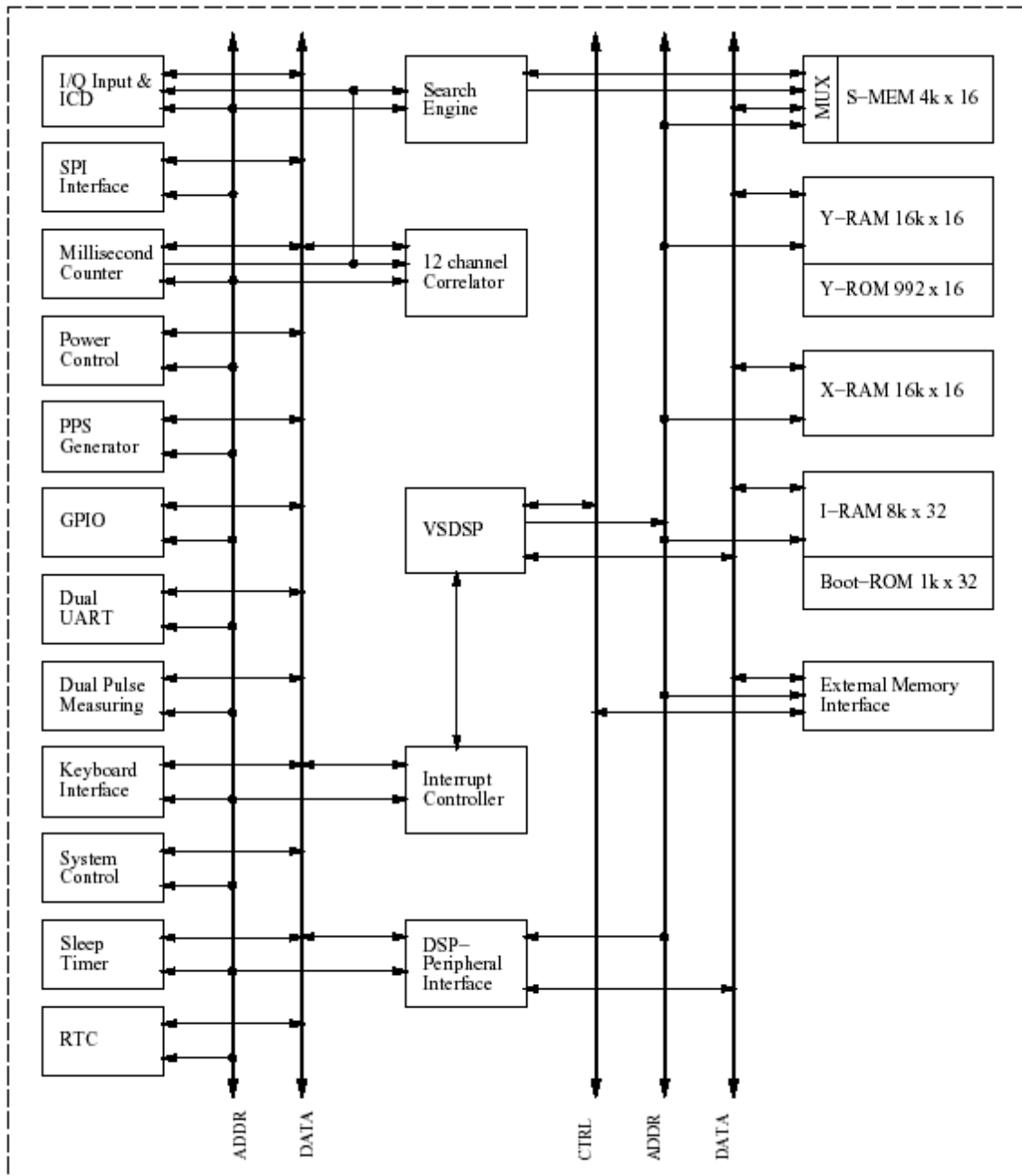


Figure 2 uN8031B Block Diagram

Pin Description

The pin description for the uN8031B defined for the STPBGA144 package is in table 1 below and the ball definition later in table 2:

Group	Name	Description
External Bus	D[15..0]	External data bus.
	A[19..0]	External address bus.
	XCS[3..0]	Active low chip select outputs.
	XWT	Active low asynchronous wait state request for external bus. Can be left unconnected when not used.
	XWR	Active low write strobe for external bus.
Control	XRD	Active low read strobe for external bus.
	RF SEL	Must be tied to DVDD
	MCLK	Master clock input (16.3676 MHz).
	XRESET	Active low asynchronous system reset input.
	RFEN	Enable/power-down signal to the external RF front-end.
Real time clock	RTC_XIN	RTC (Real Time Clock) XTAL oscillator input pin (32768 Hz).
	RTC_XOUT	RTC XTAL oscillator output pin (32768 Hz).
	XVDD	Analog power for the real time clock oscillator.
RF Front-end	ISIGN	In-phase arm IF signal sign input.
	IMAGN	In-phase arm IF signal magnitude input.
	QSIGN	Quadrature arm IF signal sign input.
	QMAGN	Quadrature arm IF signal magnitude input.
SPI Interface	SCK	Serial clock output for SPI interfaced chips
	SPI_XCS0	Chip select (active low) to SPI chip 0 (EEPROM).
	SPI_XCS1	Chip select (active low) to SPI chip 1 (external RF)
	SPI_SDI	Serial data input from SPI interfaced chips.
	SPI_SDO	Serial data output to SPI interfaced chips.
Peripherals	RXD0	CMOS level asynchronous input for UART port #0. Can be left unconnected when not used.
	TXD0	CMOS level asynchronous output for UART port #0.
	RXD1	CMOS level asynchronous input for UART port #1. Can be left unconnected when not used.
	TXD1	CMOS level asynchronous output for UART port #1.
	PPS	1PPS signal output.
	PM0	Input for pulse measurement 0. Can be left

		unconnected when not used.
	PM1	Input for pulse measurement 1. Can be left unconnected when not used.
	GPIO[15..0]	Interrupt-capable general-purpose IO pins. Can be left unconnected when not used.
	KBDOUT[4..0]	Keyboard controller row select outputs.
	KBDIN[4..0]	Keyboard controller column inputs. Can be left unconnected when not used.
Test	TEST	Active high test mode select input. Connect to GND for normal operation.
	TEST[12..0]	Miscellaneous test pins. Connect all to GND for normal operation. Other test pins are shared with GPIO.
Power	DVDD	Pad and core power. (18 pins)
	GND	Pad and core ground. (20 pins)

Table 1. uN8031B Pin Description

A1 TEST[0]	C1 DVDD	E1 D[11]	G1 DVDD	J1 D[2]	L1 DVDD
A2 TEST[1]	C2 DVDD	E2 D[13]	G2 D[7]	J2 D[3]	L2 XCS1
A3 TEST[2]	C3 RFEN	E3 D[15]	G3 D[8]	J3 D[1]	L3 XCS2
A4 TEST[3]	C4 TEST[8]	E4 D[12]	G4 GND	J4 A[0]	L4 A[1]
A5 XVDD	C5 TEST[9]	E5 TEST[12]	G5 GND	J5 A[6]	L5 A[4]
A6 SPI_XCS1	C6 RTC_XIN	E6 GND	G6 GND	J6 GND	L6 A[7]
A7 MCLK	C7 RF_SEL	E7 GND	G7 GND	J7 GND	L7 A[11]
A8 DVDD	C8 SPI_SDO	E8 GPIO[0]	G8 GND	J8 A[16]	L8 A[14]
A9 ISIGN	C9 QMAGN	E9 GPIO[4]	G9 GND	J9 KBDOUT[3]	L9 A[17]
A10 KBDIN[0]	C10 TXD1	E10 GPIO[6]	G10 GPIO[10]	J10 TXD0	L10 KBDOUT[0]
A11 KBDIN[1]	C11 DVDD	E11 GPIO[5]	G11 GPIO[11]	J11 DVDD	L11 KBDOUT[4]
A12 PM0	C12 RXD1	E12 DVDD	G12 GPIO[9]	J12 DVDD	L12 KBDIN[4]
B1 TEST[4]	D1 D[14]	F1 DVDD	H1 D[6]	K1 DVDD	M1 XCS0
B2 DVDD	D2 XWT	F2 D[10]	H2 D[5]	K2 XRD	M2 A[2]
B3 TEST[5]	D3 PPS	F3 D[9]	H3 D[4]	K3 XWR	M3 DVDD
B4 TEST[6]	D4 TEST[10]	F4 GND	H4 D[0]	K4 XCS3	M4 A[5]
B5 TEST[7]	D5 TEST[11]	F5 GND	H5 A[9]	K5 A[3]	M5 A[8]
B6 RTC_XOUT	D6 GND	F6 GND	H6 GND	K6 XRESET	M6 A[10]
B7 SPI_SCK	D7 GND	F7 GND	H7 GND	K7 A[12]	M7 A[13]
B8 SPI_SDI	D8 SPI_XCS0	F8 GND	H8 RXD0	K8 A[15]	M8 DVDD
B9 IMAGN	D9 QSIGN	F9 GND	H9 GPIO[13]	K9 A[18]	M9 A[19]
B10 DVDD	D10 GPIO[1]	F10 GPIO[8]	H10 GPIO[15]	K10 KBDOUT[1]	M10 KBDOUT[2]
B11 DVDD	D11 GPIO[2]	F11 GPIO[7]	H11 GPIO[14]	K11 TEST	M11 KBDIN[3]
B12 PM1	D12 GPIO[3]	F12 DVDD	H12 GPIO[12]	K12 DVDD	M12 KBDIN[2]

Table 2. uN8031B Package STPBGA Definition

Some of the pads of *uN8031B* include a pull-up or a pull-down resistor or a keeper; therefore no external resistor is required. If not used, the pins connected to these pins can be left unconnected. For keeper pins with resistive straps, 4.7K ohms is recommended to insure sufficient current to change state. The following table lists these special pins:

Pin	Pad Type
D[15..0]	keeper
GPIO[15..0]	keeper
PM0	keeper
PM1	keeper
KBDIN[4..0]	100kΩ pull-down
XWT	100kΩ pull-up
RXD0	100kΩ pull-up
RXD1	100kΩ pull-up
SPI_SDI	10kΩ pull-up

Table 3. Pin Types

Interconnection with uN8021B

The *uN8021B* external GPS RF front-end chip can be connected to *uN8031B* GPS baseband processing chip using 10 signals as shown in the figure below. No external glue logic or pull-up/pull-down resistors are required. The signals can be divided into three separate function groups as follows:

- System signals (clock, reset, RF enable)
- Data signals from RF to baseband (I/Q sign and magnitude)
- Control signals from baseband to RF (SPI interface)

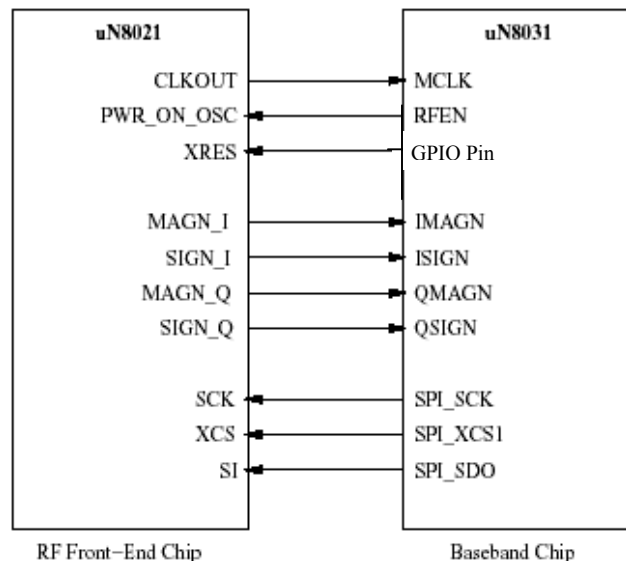


Figure 3. Interconnection Diagram with uN8021B

General Description

The *uN8031B* GPS Baseband Receiver implements hardware necessary for acquiring and tracking GPS satellite signals as well as enough processing capability and memory for on-chip navigation solution computation. It is based on u-Nav's extensive GPS design experience.

The *uN8031B* GPS Baseband Receiver has two main functional units for GPS signal processing: dedicated acquisition unit based on QwikLock™ search engine technology and a hardware correlator based tracking unit employing Zoom Correlators™. These are controlled by a proprietary low-power DSP processor core referred to in this document as the VS_DSP. The chip has integrated program and data memories for the software and data, and interfaces to the application system via two asynchronous serial ports. There is an external memory bus for connecting non-volatile FLASH memory which will hold the DSP software and any necessary non-volatile storage requiring data. There is also a 16-pin general purpose I/O interface which enables interfacing the uN8031B to many other devices. The 1PPS output is capable of delivering an accurate time mark signal if required by the application. The *uN8031B* has extensive and flexible power control which enables extremely low-power GPS receiver operation. This is required by many portable applications where power is at premium. Even with low-power operation, the *uN8031B* still has high performance.

Chip Clocks and Reset

The chip clocking is shown in figure 3. The clock frequency is doubled internally and the DSP generates two clocks from it: CLK and INTCLK. The CLK is used by VS_DSP and memories. It is stopped in HALT-state or when a wait-state is requested by external bus interface or peripherals. The INTCLK is used by the search engine, correlator and peripherals. It is not affected by HALT-state or wait-states. During the SLEEP-state the clock doubler does not generate clock. The clock doubler has a counter which is used at power-up and when the SLEEP-state is ended. The counter gives 4096 clock cycles time for the input clock to stabilize before it is driven out of clock doubler.

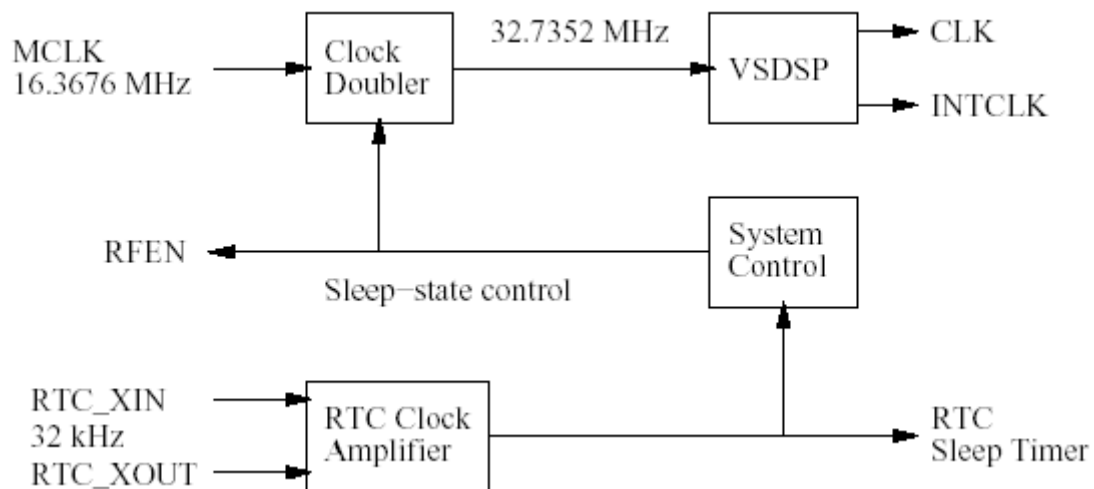


Figure 4. uN8031B Clocking

There is also another clock, the real time clock or RTC, which is generated from the RTC_XIN/RTC_XOUT pair and is used for system control and very low power peripherals (RTC/sleep timer). The reset input XRESET is active low and should have an external power-on reset circuit.

Interfaces

The intermediate frequency (IF) input from the RF front-end chip comes to the *uN8031B* as a pair of two-bit digital signals. It is interpreted as a complex number consisting of real and imaginary parts, corresponding to the In-phase and Quadrature arms of the signal. The IF nominal frequency is around 40 kHz.

The 16-bit external memory bus is compatible with most asynchronous SRAM and FLASH memories allowing direct connection of the memories to the bus. There are four pre-decoded active-low chip-select signals for connecting up to four different devices to the bus. The bus is capable of accessing one megaword (20-bit address) on each of the four devices. In order to interface flexibly with external memories having different speeds, the external data bus has configurable wait states.

The external data bus interface multiplexes VS_DSP core buses XDB, YDB and IDB to the external (off-chip) data bus EDB. 32-bit wide IDB accesses are converted to two 16-bit EDB accesses.

There are other peripheral devices in the *uN8031B* in addition to the dedicated GPS receiver blocks:

- 2 x UART
- 1PPS pulse generator
- SPI interface to 2 external devices (such as a boot-EEPROM and external *uN8021B* RF front-end)
- 16 bit parallel I/O which are capable of generating interrupts
- IF signal bit counter
- 16-bit millisecond counter
- 32-bit interrupt controller
- 24-bit real time clock
- 16-bit sleep timer
- 10-bit keyboard interface
- 2 pulse measurement units
- PowerMiser™ power controller

The peripherals are controllable by the VS_DSP through a memory mapped register interface.

Functional Units

There are three main functional units on the *uN8031B*: the search engine (a dedicated acquisition unit based on QwikLock™ technology), the hardware correlator based

tracking unit employing Zoom Correlators™, and the proprietary low-power VS_DSP processor core. In addition there are a number of peripheral units as well as the integrated memory required for the GPS algorithm implementation.

Search Engine

The Search Engine is a u-Nav Microelectronics developed rapid acquisition block. The search engine block implements the acquisition time frequency analysis and signal integration and it has the following main features:

- 2-bit I/Q inputs
- 2046 sample time axis giving 1/2 chip resolution
- Programmable Doppler frequency
- Pre-detection integration time: 1–32 ms
- Post-detection integration rounds: 1–32
- On-chip dedicated integration memory, accessible also by the VS_DSP
- Can be synchronized to known bit timing
- Autonomous operation, generates interrupt upon completion

Correlator Unit

The correlator unit implements the hardware for baseband tracking through 12 parallel hardware correlation channels using Zoom Correlators™. The main features of the correlator unit are:

- 2-bit I/Q inputs
- 12 parallel tracking channels
- 4 Zoom Correlators™ per tracking channel
- Individual channels can be enabled or disabled for saving power
- Easy setting of tracking state for rapid signal acquisition
- Mixed individual and common dump: All channel output data is sampled synchronized to that channel's code generator epoch timing, one interrupt is generated with an interrupt source register indicating the channel which generated the interrupt. All measurement data (code and carrier counts and phases) is sampled simultaneously for all channels. Only one interrupt is generated. The dump rate is settable via a counter.

VS_DSP Architectural Description

The VS_DSP is the VLSI Solution proprietary VS_DSP processor core described in the *VS_DSP User's Manual*. The processor implementation within the uN8031B is generated with the architecture listed below:

- Data word, data address, and program address widths are 16 bits
- Program word width is 32 bits
- Multiplier input is 16 bits with eight accumulator overflow guard bits
- Eight arithmetic registers and eight index registers
- One hardware loop mechanism
- Version 2 instruction set with paging

Code and Data Memory

The code and data memories are the dedicated VS_DSP memories required for the proper implementation of any GPS software to be run on the VS_DSP processor. The internal memories include the following blocks:

- 16K 16 bit wide words X-bus data RAM memory
- 16K 16 bit wide words Y-bus data RAM memory
- 4K 16 bit wide words Y-bus data RAM (S-mem) also by the search engine
- 8K 32 bit wide words of Program RAM memory
- 992 16 bit wide words of Y-data ROM
- 1 K 32 bit wide words Boot ROM memory

Paged accesses to external memory areas are handled by the external bus interface. Externally the *uN8031B* can address up to 4M 16 bit words of data or program memory.

Power Controller

The *uN8031B* can reduce power consumption by disabling individual peripheral devices and halting the VS_DSP. In the halt-state the VS_DSP and memories are not clocked, but the peripherals are clocked and can wake up the VS_DSP by generating an interrupt. When a peripheral device is disabled its registers can be read but not written.

Further power saving can be achieved by disabling the master clock and changing to the SLEEP state. During SLEEP-state only the system control, RTC and sleep timer are clocked with special 32768Hz clock. Leaving the SLEEP-state can be triggered by RTC, sleep timer, keyboard or GPIO.

Millisecond counter

The millisecond counter generates one epoch pulse every 32736th clock cycle (near millisecond with 32.735MHz internal clock). The epoch pulse is used by the VS_DSP (INT_TIMER interrupt), search engine, correlator and 1PPS unit for synchronization. The millisecond counter peripheral also has a 16-bit counter which counts the number of epoch pulses.

PPS Signal Generator

The PPS is a 15-bit counter which starts counting from a configured value down to 0 after a millisecond pulse is received. When 0 is reached, a new value for PPS output is fetched from a configuration register.

SPI Interface

The SPI interface has two chip select signals enabling two external SPI-compliant chips to connect to *uN8031B*. The SPI_XCS0 chip select should be connected to a serial EEPROM which can be used as an external boot-up memory device. SPI_XCS1 is typically used for controlling an external RF chip. Only one chip at a time can use the interface. The *uN8031B* chip acts as a master device and is controlled through memory mapped register interface.

The SPI clock speed can be 2Mhz, 1Mhz, 500kHz or 250kHz. Four EEPROM read and write modes are supported: read data, write data, read status and write status. Note that the SPI_SDI pin does not require an external pull-up to prevent the pin from floating, if no external SPI device is active or there are no external SPI devices, since there is an internal pull-up on the pad. The pull-up capability and thus the speed of the interface can be increased using an external pull-up resistor smaller than the 10kΩ on-chip resistor.

If only the external RF chip is connected to the SPI interface, the connections are made as shown in figure 3 earlier and the SPI_SDI pin can be left unconnected. If the serial EEPROM is also connected, the SPI connections should be made as shown in figure 5 below where a 25LC640 serial EEPROM is used as an example:

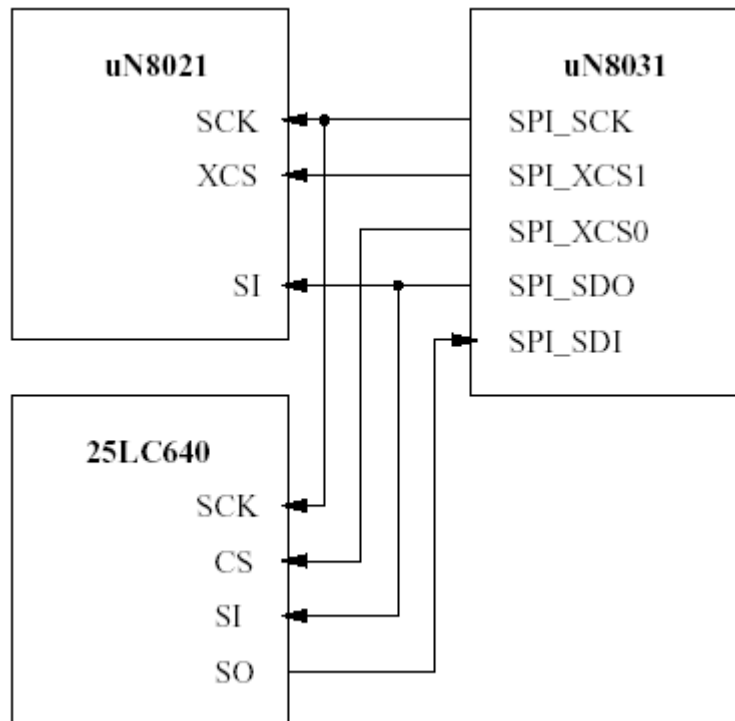


Figure 5: SPI with RF and EEPROM chips

IF Signal Bit Counter Device (ICD)

The ICD block counts ones in sign and magnitude bits of incoming I and Q signal in a given time interval. The values are used in configuring the gain parameter in the RF front end. After the given time interval has elapsed, the block generates an INT ICD interrupt and four 16 bit values are readable through memory mapped register interface.

Dual UART

These two identical peripherals implement serial interfaces using RS232 data format with CMOS signal levels. Both interfaces include transmit and receive functions at the speed of 300 bps and higher. After the reset, the communication speed is initialized to 9600 bps, if the input clock speed is 16.3676 MHz. Other speeds can be achieved by writing new

clock divider values to the device using the processor. The only data format supported by the UARTs is 8 bit data with one stop bit and no parity.

Real Time Clock

The real time clock (RTC) increments a 24-bit up counter 256 times in a second. It has a 24-bit alarm register which can be used to generate RTC alarms. The RTC is clocked with a special 256 Hz clock (generated from the 32768 Hz clock input) giving 3.9 ms accuracy for alarms. Reset has no effect on RTC counter, neither has the processor clock/SLEEP state since the RTC is clocked by different clock. The value of RTC counter is undefined after power up.

The RTC unit has a clock crystal input and output pins and its own power supply pin, XVDD. The connection diagram for the RTC pins is shown in figure 6. Check the datasheet of the crystal oscillator for the correct capacitance values.

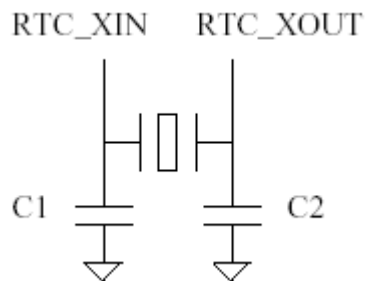


Figure 6: Connecting the RTC Crystal pins

Sleep timer

The sleep timer is a 16-bit down counter which has a resolution of 7.8 ms (128 Hz). It generates an INT SLEEP interrupt when it reaches zero. It can be also be used to wake the *uN8031B* from the SLEEP state.

Interrupt Controller

The interrupt controller delivers the interrupt requests from the peripherals to the processor. Each interrupt source has own interrupt vector (interrupt handler start address). There are three levels of priority and a disable/enable mask available for all the sources.

Pulse measurement interface

The *uN8031B* has two pulse measurement devices, which can be used to measure with great accuracy how long an input stays high or low. The pulse measurement devices support several accuracy modes, trigger modes (once-only, continuous-wait and continuous) and input polarity.

Keyboard I/O Port

The keyboard controller can be connected to up to 5x5 keyboard matrix. The controller scans the matrix and generates an interrupt (INT KBD) when a key is pressed or released. There is bounce-removal logic with a 28 ms delay time. The controller does not support

cases where multiple keys are pressed simultaneously. The connection of a full keyboard switch matrix is illustrated in Fig. 7. The pull-down resistors are required on all input pins if a keyboard is connected. If any of the KBDIN-pins is not needed, they can be left unconnected since there is an internal 100kΩ pull-down. Thus if no keyboard is to be used, no external components need to be connected to the keyboard I/O port.

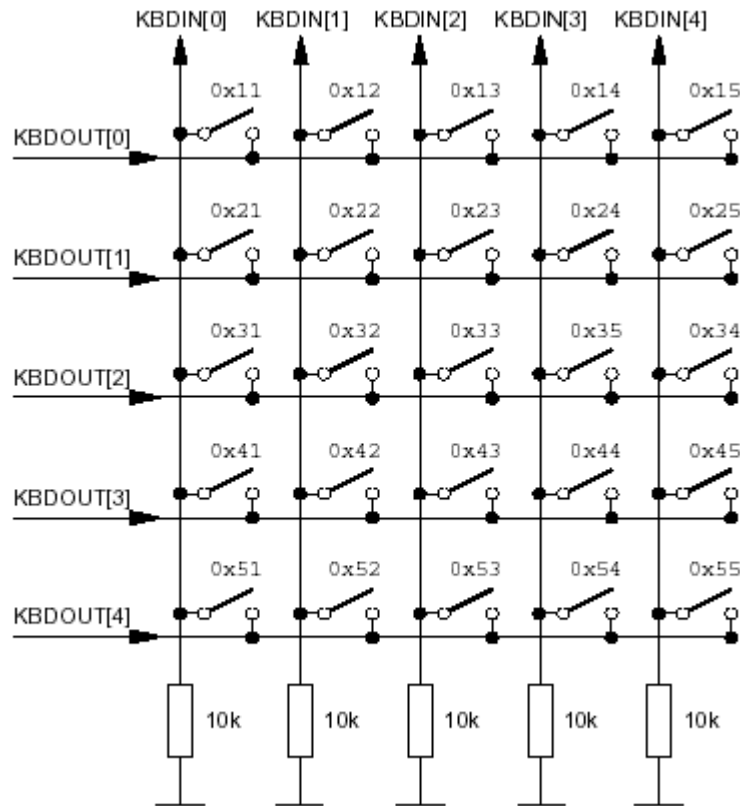


Figure 7: Connection of a full 5x5 keyboard matrix

The timing diagram of the keyboard I/O port is shown in figure 8.

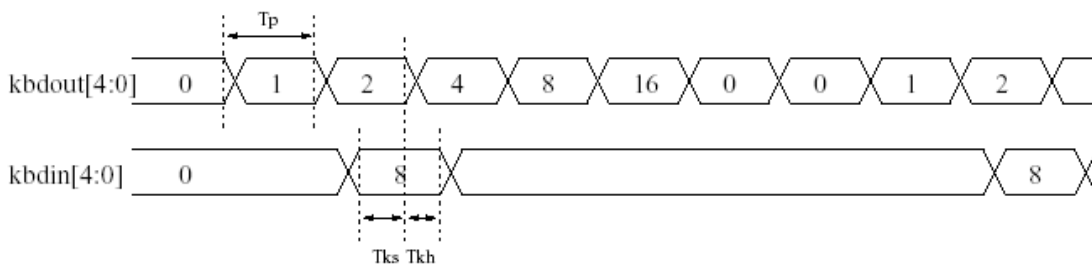


Figure 8: Keyboard I/O port timing

Each row (connected to KBDOUT) is pulled to logic one during its scan turn and each column (connected to KBDIN) is read during this scan. Each complete scan takes seven scan cycles of length T_p , which is 512 times the master clock cycle length. The master clock is twice the system input clock, therefore being approximately 32 MHz. If the scan

result (in this example bit 3 for row 1, because KBDOUT[4..0] was driven to 00010 and KBDIN was 01000) stays the same during 256 consecutive scans (28 ms real time), it is considered valid. This creates the bounce-removal action. The data is sampled at the end of the scan cycle. The setup time T_{ks} and the hold time T_{kh} is 10 ns or more.

Parallel I/O Port

The Parallel I/O port (GPIO) is 16-bit input/output interface, on which each bit can be configured as input or output. The GPIO can be used to connect different kinds of peripherals such as an LCD-display to the *uN8031B*. If a bit is configured as input, it can be configured to generate an interrupt (INT GPIO) as well. Interrupt can be configured to happen on rising, falling or on both edges of the input signal.

Since the two MSBs of the GPIO port (bits 14 and 15) are used by the internal ROM in selecting the boot-up source, they must be pulled either to GND or DVDD through resistors and are generally not usable for other purposes. The boot-up source is selected by the following logic:

Bit 15	Bit 14	Source
0	0	SPI device 0
0	1	UART 0
1	0	External memory
1	1	External memory

Table 4. Configuring Boot Source

External Bus Interface

The external bus interface multiplexes core buses XDB, YDB and IDB to the external (off-chip) bus EDB. 32-bit IDB accesses are converted to 16-bit EDB accesses. In order to interface flexibly with external memories having different speeds, EDB has configurable wait states.

The external bus has four programmable chip select outputs for external memory blocks. All four chip select output can have different amounts of wait states. In addition to this, wait states can be requested asynchronously using the XWT input pin. Chip select outputs XCS[3:0] are active low.

Addresses

Logical addresses are converted to physical addresses by the external bus interface to map all three address spaces (X, Y and I) to a single address space (E).

For external X addresses, the physical address is the logical address. For external Y addresses, the physical address is obtained by inverting logical address bit 15. This maps the Y addresses to the “gap” left by internal X data space ending at 0x8000. For external I addresses, the physical address is obtained as follows:

1. The logical address is inverted.
2. The inverted address is shifted left by 1 bit.
3. The LSB is set to 0 for low 16 bit access or to 1 for high 16 bit access.

This maps the zero-page (first 64K) instruction addresses to end of external memory.

The above scheme allows both data and instruction to reside in same physical memory. Data is in the start of the memory and instructions in the end of the memory. The mapping is conceptually depicted in figure 9. This shows how I:0x0000 would be mapped to external E:0xffff ffff and E:0xffff fffe, I:0x0001 to E:0xffff fffd and E:0xffff fffc and so on. External Y-memory range Y:0x8000 to Y:0xffff is mapped to E:0x0000 to E:0x7fff. Because of internal on-chip instruction memory, the external memory from I:0x00000 through I:0x023FF is not actually accessible as instruction memory as suggested in the figure below. Instead, this space is accessible only as X memory.

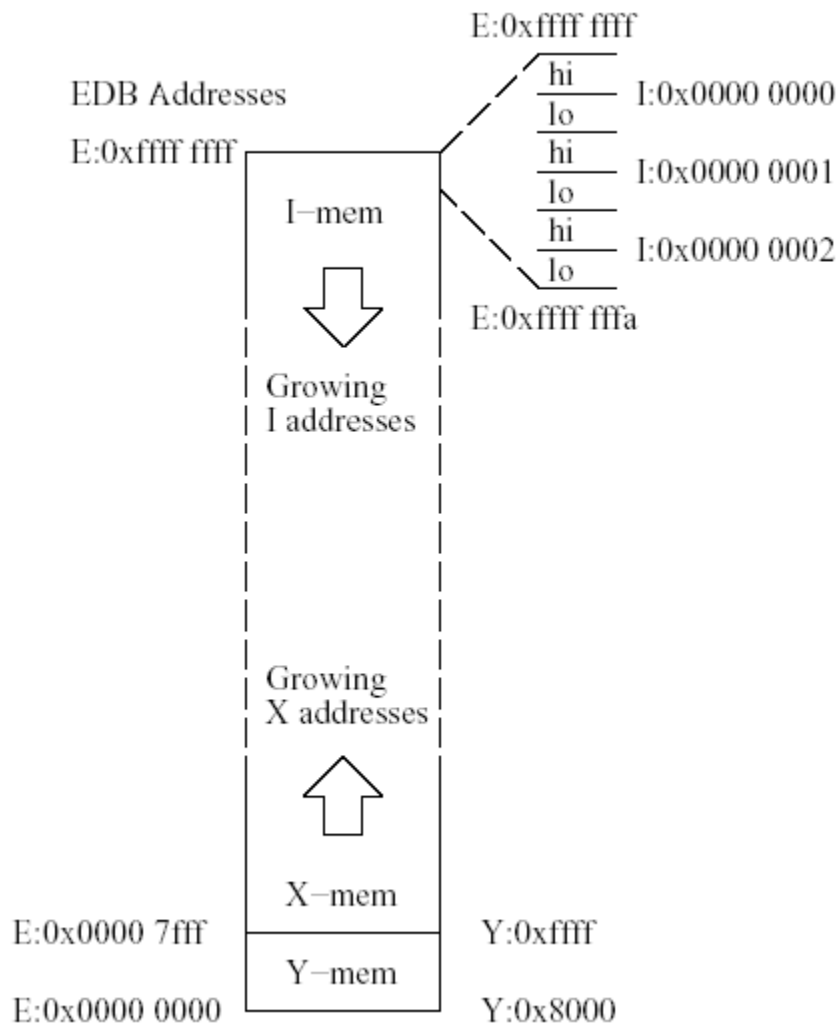


Figure 9. Internal to External Memory Space Mapping

Register Programming

Refer to the uN8031 User's Manual for detailed information on all uN8031B programmable registers except EDB configuration. The following sections provide a detailed description of only those registers configuring the external data bus.

External Data Bus Configuration Registers

The external data bus interface is controlled by two registers, bus control register (BCR0) and chip select register (BCR1). They are mapped to internal data memory as follows:

Address	Name	Type	Width	Format
0x4000	BCR0	R/W	16	bit field
0x4001	BCR1	R/W	4	bit field

Table 6. External Bus Configuration Registers

The external bus interface control register BCR0 is used to configure the wait states. Each chip select output XCS[3..0] has four programmable bits which contain the number of wait states to be generated for that chipselect output. Each wait state corresponds to one clock cycle. The bits are located in BCR0 as follows:

Bits	Description
15..12	XCS[3] wait states
11..8	XCS[2] wait states
7..4	XCS[1] wait states
3..0	XCS[0] wait states

Table 7. Register BCR0 Bit Definition

At reset, BCR0 is initialized to all ones. This selects a default of 15 wait states for all external memory accesses. Figure 10 illustrates a write operation with wait states. In read operations the read signal XRD has similar timing as XWR. Clocks are not part of the interface but they are included here to show how EDB access is synchronized to core clocks.

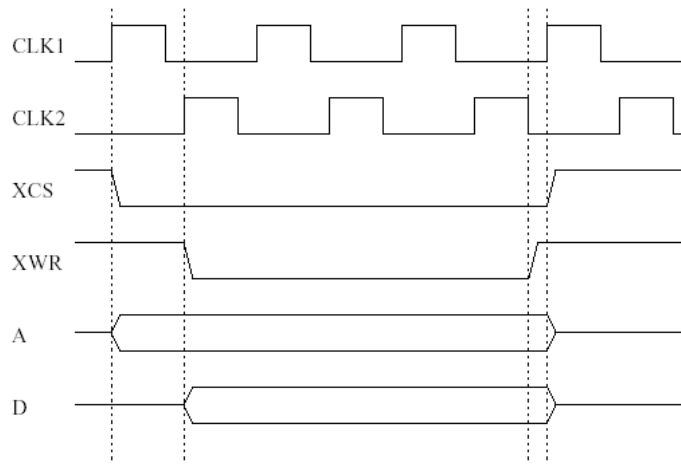


Figure 10. EDB timing

The chip select register BCR1 is used to configure the behavior of the four chip select outputs. These bits are defined as follows:

Bits	Description
3	Must be programmed to zero
2	Y peripheral enable
1	XCS[0] includes BL3
0	CS block size

Table 8. Register BCR1 Bit Definition

External memory is divided into four blocks of equal size being either 4MW or 16MW. BCR1 bit 0 selects the memory block size. If the bit is 0, block size is 4MW. If the bit is 1, block size is 16MW. 16MW block size is default at boot-up but typically is reconfigured to 4MW. The corresponding memory blocks (address ranges) are shown in table 9 where “X” denotes data and “I” instruction address ranges. Block decoding in 4MW mode is determined by logical address bits 23 and 22 with bits 31..24 don’t care. Block decoding in 16MW mode is determined by logical bits 25 and 24 with bits 31..26 don’t care. Table 9 sets the upper don’t care bits to zero for clarity.

The *uN8031B* physically has only 20 least significant bits of the address connected externally making the native block size 1MW. Table 10 shows example address ranges which could be used in 4M block size mode. There are several other possible choices (the 1M block is visible in four different places within a 4M block) but this one provides continuous memory between BL0–BL1 and BL2–BL3.

Block	4M block size	16M block size
BL0	X 0x0000 0000 ... 0x003F FFFF I 0x0060 0000 ... 0x007F FFFF	X 0x0000 0000 ... 0x00FF FFFF I 0x0180 0000 ... 0x01FF FFFF
BL1	X 0x0040 0000 ... 0x007F FFFF I 0x0040 0000 ... 0x005F FFFF	X 0x0100 0000 ... 0x01FF FFFF I 0x0100 0000 ... 0x017F FFFF
BL2	X 0x0080 0000 ... 0x00BF FFFF I 0x0020 0000 ... 0x003F FFFF	X 0x0200 0000 ... 0x02FF FFFF I 0x0080 0000 ... 0x00FF FFFF
BL3	X 0x00C0 0000 ... 0x00FF FFFF I 0x0000 0000 ... 0x001F FFFF	X 0x0300 0000 ... 0x03FF FFFF I 0x0000 0000 ... 0x007F FFFF

Table 9. Memory Block Address Ranges

Block	4M block size
BL0	X 0x0030 0000 ... 0x003F FFFF I 0x0060 0000 ... 0x0067 FFFF
BL1	X 0x0040 0000 ... 0x004F FFFF I 0x0058 0000 ... 0x005F FFFF
BL2	X 0x00B0 0000 ... 0x00BF FFFF I 0x0020 0000 ... 0x0027 FFFF
BL3	X 0x00C0 0000 ... 0x00CF FFFF I 0x0008 0000 ... 0x001F FFFF

Table 10. Example Memory Address Ranges for 4M Block Size

BCR1 bit 1 includes BL3 for chip select XCS[0]. This can be used if a single memory device is used for both data and program memory.

BCR1 bit 2 enables chip select for external Y peripherals. If the bit is 0, then external Y peripheral accesses are mapped to normal Y data memory chip select. If the bit is 1, then external Y peripheral accesses are separated from Y data accesses.

Chip select outputs function as follows:

XCS[0]	Active in accesses to BL0. if BCR1 bit 1 is 1, active also in accesses to BL3.
XCS[1]	Active in accesses to BL1.
XCS[2]	If BCR1 bit 2 is 0, active in accesses to BL2. If BCR1 bit 2 is 1, active for Y peripheral accesses.
XCS[3]	Active in accesses to BL3.

Table 11. Chip Select Mapping

Note that if BCR1 bit 1 is 1, both XCS[0] and XCS[3] will be active in BL3 accesses. In this case, it is advisable to leave XCS[3] unused.

Also note that if BCR1 bit 2 is 1, BL2 will not be available. All accesses to BL2 will most probably result in data corruption and/or program crash.

BCR1 bit 3, when 1, enables VS DSP #1 compatibility mode. This bit must be programmed 0 for normal operation in the uN8031B.

The mapping of chip select signals to external X-memory blocks with different BCR1 settings is shown in figure 11. Each block contains four address ranges denoting the images of the same memory space. The address range visible on the external bus is 0x00000...0xfffff for each of the 16 address ranges. For addresses larger than 24 bits, the 8 most significant bits are effectively don't care so the mapping depicted in the figure will be repeated through the 32-bit address space.

The mapping of chip select signals to instruction I-memory blocks is shown in figure 12.

		BCR1	0000	0010	0100	0110
BL0	X:0x0000 0000 . . . 0x000F FFFF					
	X:0x0010 0000 . . . 0x001F FFFF	XCS0	XCS0	XCS0	XCS0	
	X:0x0020 0000 . . . 0x002F FFFF					
	X:0x0030 0000 . . . 0x003F FFFF					
BL1	X:0x0040 0000 . . . 0x004F FFFF					
	X:0x0050 0000 . . . 0x005F FFFF	XCS1	XCS1	XCS1	XCS1	
	X:0x0060 0000 . . . 0x006F FFFF					
	X:0x0070 0000 . . . 0x007F FFFF					
BL2	X:0x0080 0000 . . . 0x008F FFFF					
	X:0x0090 0000 . . . 0x009F FFFF	XCS2	XCS2	-	-	
	X:0x00A0 0000 . . . 0x00AF FFFF					
	X:0x00B0 0000 . . . 0x00BF FFFF					
BL3	X:0x00C0 0000 . . . 0x00CF FFFF		XCS0		XCS0	
	X:0x00D0 0000 . . . 0x00DF FFFF	XCS3		XCS3		
	X:0x00E0 0000 . . . 0x00EF FFFF		XCS3		XCS3	
	X:0x00F0 0000 . . . 0x00FF FFFF					

Figure 11. External X-Memory Mapping to XCS Signals

		BCR1	0000	0010	0100	0110
BL0	I:0x0078 0000 . . . 0x007F FFFF					
	I:0x0070 0000 . . . 0x0077 FFFF	XCS0	XCS0	XCS0	XCS0	
	I:0x0068 0000 . . . 0x006F FFFF					
	I:0x0060 0000 . . . 0x0067 FFFF					
BL1	I:0x0058 0000 . . . 0x005F FFFF					
	I:0x0050 0000 . . . 0x0057 FFFF	XCS1	XCS1	XCS1	XCS1	
	I:0x0048 0000 . . . 0x004F FFFF					
	I:0x0040 0000 . . . 0x0047 FFFF					
BL2	I:0x0038 0000 . . . 0x003F FFFF					
	I:0x0030 0000 . . . 0x0037 FFFF	XCS2	XCS2	-	-	
	I:0x0028 0000 . . . 0x002F FFFF					
	I:0x0020 0000 . . . 0x0027 FFFF					
BL3	I:0x0018 0000 . . . 0x001F FFFF		XCS0		XCS0	
	I:0x0010 0000 . . . 0x0017 FFFF	XCS3		XCS3		
	I:0x0008 0000 . . . 0x000F FFFF		XCS3		XCS3	
	I:0x0000 0000 . . . 0x0007 FFFF					

Figure 12. External I-Memory Mapping to XCS Signals

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Storage temperature range	T_{STG}	-55	+150	°C
Operating temperature range	T_A	-30	+85	°C
Maximum power dissipation ($T_A = +85\text{ °C}$)	P_D		500	mW
Current on any pin to avoid latch-up	I_{MAX}	-30	+30	mA
ESD protection	V_{ESD}	2000		V
Supply voltage, digital	DVDD	-0.3	3.6	V
Supply voltage, RTC	XVDD	-0.3	3.6	V
Input pin voltage, I/O	V_{IO}	-0.3	DVDD+0.3	V

Table 14. Absolute Maximum Ratings

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Item	Symbol	Min	Typical	Max	Unit
Operating temperature	T_A	-30		+85	°C
Supply voltage, digital	DVDD	2.7	3.0	3.3	V
Supply voltage, RTC (Recommended to be same level as DVDD.)	XVDD	2.7	3.0	3.3	V

Table 15. Recommended Operating Conditions

Digital Signal Characteristics

Item	Symbol	Test Condition	Min	Max	Unit
Input high voltage	V_{IH}		0.7xDVDD	DVDD+0.3	V
Input low voltage	V_{IL}		-0.3	0.3xDVDD	V
Output high voltage	V_{OH}	$I_{OH} = 1\text{mA}$	0.8xDVDD	DVDD	V
Output low voltage	V_{OL}	$I_{OL} = -1\text{mA}$	0	0.22xDVDD	V
Input leakage (Not applicable to pins in Table 3 with keeper or resistive strap.)	I_{LI}	25 °C	-5.0	+5.0	μA

Table 16. Digital DC Characteristics

Item	Symbol	Min	Typical	Max	Unit
Clock frequency, MCLK	F_c	16.36675	16.3676 ^{note 1}	16.36794	MHz
Clock period, MCLK	t_C		61 ^{note 2}		ns
Clock duty cycle ³	t_{DUTY}	45		55	%
Digital input pin capacitance	C_i			3	pF
Digital output load capacitance	C_L			20	pF

Table 17. Digital AC Characteristics

¹ The constraints on MCLK frequency correspond to IF frequencies ranging between 5 KHz and 120 KHz.

² Note that the RF oscillator frequency must be 16.3676 MHz, so the 61 ns clock cycle is not exact.

³ MCLK duty cycle must be within these specifications to insure proper on-chip clock doubling operation.

Typical Operating Power

Operating power consumption is mode and software dependent. Some representative numbers are given in the table below:

Mode	Description	Conditions	Typical	Unit
Search	Signal acquisition with Search Engine running continuously and 8 channels tracking	DVDD = 3.0V 25 °C	58	mW
Run	Tracking 8 channels with Search Engine running 10% of the time.	DVDD = 3.0V 25 °C	35	mW
Sleep	Only RTC running	DVDD = 3.0V 25 °C	0.03	mW

Table 18. Typical Modal Operating Power

In both the *search* and *run* situations, eight correlator channels are active. The number of active channels affects the power consumption. The actual power consumption depends also on the peripheral device activity which is application-specific. A more detailed description on operating currents and power consumption behavior of the *uN8031B* can be found in the User’s Manual in subsection “Power Consumption”.

Digital Timing

The external bus timing diagram is illustrated in the figure below. Note that the chip select signals (XCS0..3) have the same timing requirements as the address signals.

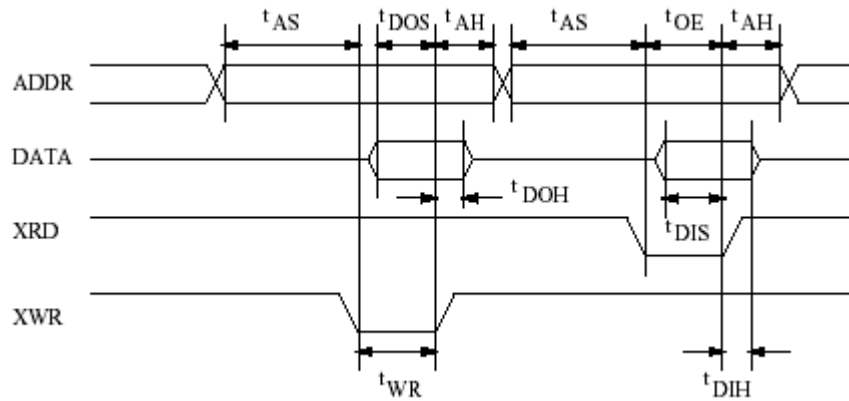


Figure 13. External Bus Timing

Item	Symbol	Min	Typical	Max	Unit
Address setup time	t_{AS}		7		ns
Address hold time	t_{AH}	2			ns
Write signal pulse width	t_{WR}		$\frac{1}{2} * (WS + 0.5) \times t_C$		ns
Read signal pulse width	t_{RD}		$\frac{1}{2} * (WS + 0.5) \times t_C$		ns
Data output setup time	t_{DOS}		$\frac{1}{2} * (WS + 0.5) \times t_C$		ns
Data output hold time	t_{DOH}	3			ns
Data input setup time	t_{DIS}	10			ns
Data input hold time	t_{DIH}	1			ns

Table 19. Recommended Operating Conditions

WS is the number of wait states programmed for the bus access.

The reset timing diagram is as follows:

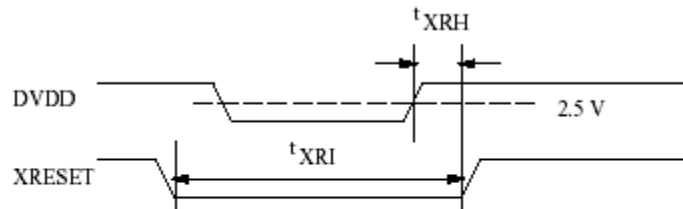


Figure 14. Reset Timing

XRESET should not be applied until after the real time clock has started and stabilized.

Item	Symbol	Min	Typical	Max	Unit
XRESET hold time	T_{XRH}	$2 \times t_C$			ns
XRESET pulse width	T_{XRI}	$2 \times t_C$			ns

Table 20. Recommended Operating Conditions

Application Notes

For best results with the uN8031B, the procedures and circuit implementations described in these application notes should be followed.

MCLK Source

The uN8031B implements an on-chip clock doubling circuit. Duty cycle variations from the ideal 50% must be minimized. TCXO reference clock sources vary in output duty cycle as a function of voltage and temperature. When using a TCXO reference source, route this clock into the uN8021B RF Front-end and derive MCLK from the RF chip CLK_OUT source. The uN8021B clock buffer will tend to self adjust the duty cycle back towards the nominal 50%. Avoid directly driving MCLK from the TCXO since this topology fails to take advantage of the self-adjusting nature in the uN8021B and may expose the uN8031B to duty cycle variation outside of the tolerated range.

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