

### Features

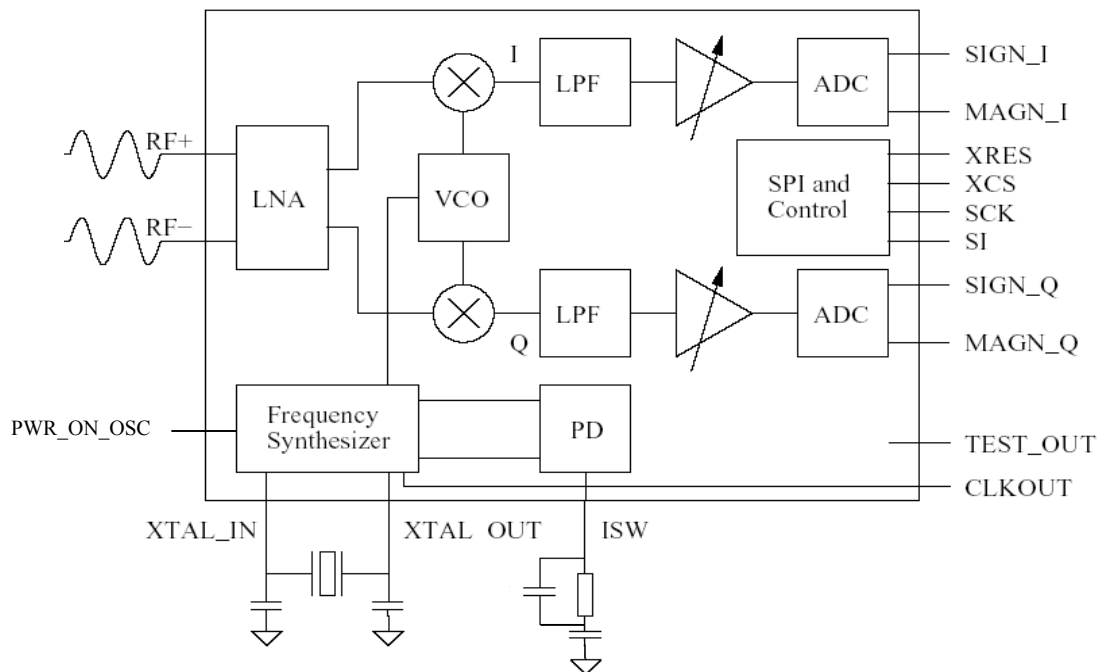
- Single-chip RF front-end for a GPS receiver
- 50  $\Omega$  balanced RF input
- Adjustable gain
- Low-power modes
- User-controllable through SPI serial interface
- 16.3676 MHz reference clock input, both crystal and external oscillator are supported
- Small area QLP-20 package, 4x4x0.9mm<sup>3</sup> size
- Glue-less interface to *uN8031A* GPS baseband receiver chip
- Level-shifted interface signals to *uN8031A*

### Description

*uN8021B* is a single-chip GPS L1 band RF front-end to be used together with a *uN8031A* GPS baseband receiver-processor chip. The *uN8021B* supercedes the *uN8021B* and contains a mixer, voltage controlled oscillator (VCO), frequency synthesizer and two analog to digital (ADC) converters. The chip can be controlled through an SPI serial interface and it is based on the direct conversion principle with on-chip filtering. It has adjustable gain and a near zero intermediate frequency (IF).

### Block Diagram

The *uN8021B* block diagram and typical analog connections below:



**Figure 1. uN8021B Block Diagram**

### Pin Description

The pin description for the uN8021B defined for the QLP-20 package is in table 1 below:

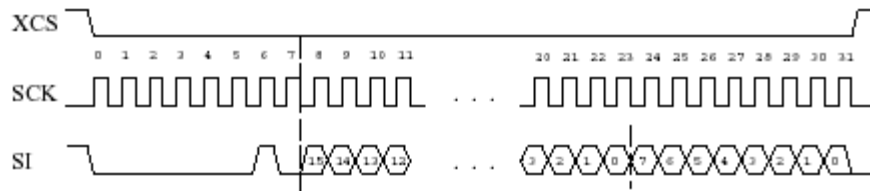
Pin #	Name	Description
1	VDD_RF_IF	Analog power for the RF I/O including XTAL_IN, XTAL_OUT, ISW, TEST_OUT, RF+, and RF- pins.
2	RF+	Positive input of differential RF-input.
3	RF-	Negative input of differential RF-input.
4	VDD_VCO	Analog power for the RF VCO block.
5	VDD_DIG	Digital power supply.
6	XTAL_IN	Crystal oscillator input pin (16.3676 MHz).
7	XTAL_OUT	Crystal oscillator output pin (16.3676 MHz).
8	TEST_OUT	I/Q arm analog output with 10 dB attenuation, $R_{out} = 1200 \Omega$
9	ISW	VCO loop filter pin.
10	PWR_ON_OSC	Enable/power-down control input for the crystal oscillator. Enables the oscillator when driven high.
11	CLKOUT	Clock output (16.3676 MHz), buffered output from crystal oscillator.
12	MAGN_I	In-phase arm IF signal magnitude output.
13	SIGN_I	In-phase arm IF signal sign output.
14	MAGN_Q	Quadrature arm IF signal magnitude output.
15	SIGN_Q	Quadrature arm IF signal sign output.
16	XRES	Active low asynchronous reset input.
17	SCK	SPI serial clock input.
18	XCS	Active low chip select.
19	SI	SPI serial data input.
20	VDD_IO	Digital I/O power supply for PWR_ON_OSC, CLKOUT, I and Q, XRES, SCK, XCS, and SI pins.
-	GND	The ground (GND), which is common to both the digital and analog parts of the chip, is not connected to any pin. Instead, the bottom of the lead frame acts as a ground connector.

**Table 1. uN8021B Pin Description**

## Register Programming

### SPI Interface

The *uN8021B* is controlled through an SPI interface. The interface contains data input only (SI pin), so the control registers can not be read. The data width (and thus the register width) is 8 bits, while the address is 16 bits. The timing of SPI interface is as follows:



**Figure 2. SPI Timing Diagram**

In the *uN8021B*, there is a total of three registers, occupying addresses 0x00 to 0x02. These registers are as follows:

Address	Name	Description
0x00	IGAIN	I-channel gain settings
0x01	QGAIN	Q-channel gain settings
0x02	CTRL	General RF control

**Table 2. uN8021B Programmable Registers**

### IGAIN and QGAIN Registers

The gain control registers IGAIN and QGAIN contain the same control bits, but IGAIN controls the I-channel gain while QGAIN controls the Q-channel. The bits of these registers are defined as follows:

Bit	Description
7	Reserved, program to 0
6	+6dB gain for the first amplifier
5	+6dB gain for the second amplifier
4	+6dB gain for the third amplifier
3	+6dB gain for the fourth amplifier
2	Bit 2 of ADC gain setting
1	Bit 1 of ADC gain setting
0	Bit 0 of ADC gain setting

**Table 3. IGAIN and QGAIN Register Definition**

The ADC gain setting (three bits with bit 2 most significant and left-most) has the following possible values:

ADC setting	Description
000	+0 dB
001	+2 dB
010	+4 dB
011	+6 dB
100	+8 dB
101	+10 dB
110	+12 dB
111	+ 14 dB

**Table 4. ADC Gain Setting Definition**

The maximum gain of +36dB is achieved by setting all bits of the gain register high. When adjusting the gain values, the best noise performance is achieved by using as high gain as possible in the first amplifier stages (control bits 6 and 5). After reset, IGAIN and QGAIN registers contain the hexadecimal value 00.

### CTRL Register

The general RF control register CTRL contains the following control bits:

Bit	Description
7	Enable I-channel test, program as 0
6	Enable Q-channel test, program as 0
5	Program as 0
4	Invert sign bit of I-channel output, effectively swaps the I- and Q-channel. Program as 0.
3	Disable frequency synthesizer clock
2	Power off VCO
1	Power off frequency synthesizer
0	Power off IF and RF

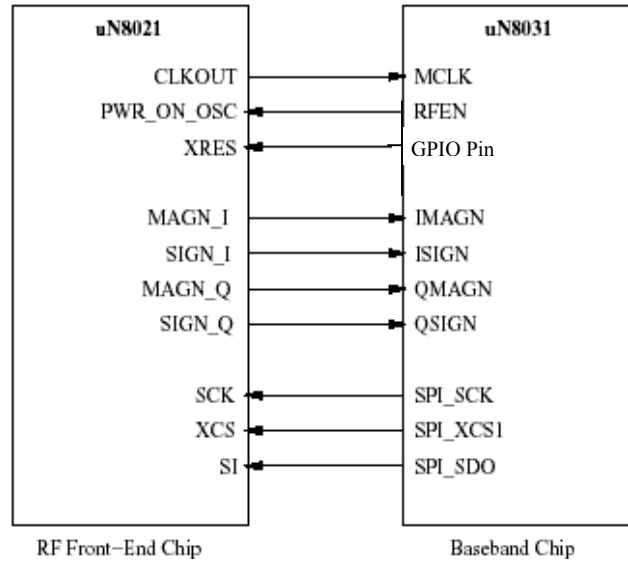
**Table 5. CTRL Register Definition**

The bits 4,5,6 and 7 are used for testing only, and should always be set to zero by the user. After reset CTRL contains the value hexadecimal 00. The chip will therefore be completely powered on.

### Interconnection with uN8031A

The *uN8021B* external GPS RF front-end chip can be connected to *uN8031A* GPS baseband processing chip using 10 signals as shown in figure 3. No external glue logic or pull-up/pull-down resistors are required. The signals can be divided into three separate function groups as follows:

- System signals (clock, reset, RF enable)
- Data signals from RF to baseband (I/Q sign and magnitude)
- Control signals from baseband to RF (SPI interface)



**Figure 3. Interconnection Diagram**

## Electrical Characteristics

### Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Storage temperature range	$T_{STG}$	-55	+150	°C
Operating temperature (ambient)	$T_A$	-30	+85	°C
Maximum power dissipation ( $T_A = +85\text{ °C}$ )	$P_D$		500	mW
Current on any pin to avoid latch-up	$I_{MAX}$	-30	+30	mA
ESD protection	$V_{ESD}$	500		V
Supply voltage, analog VDD_RF_IF and VDD_VCO	AVDD	-0.3	3.6	V
Supply voltage, digital VDD_DIG	DVDD	-0.3	3.6	V
Supply voltage, digital I/O VDD_IO	IOVDD	-0.3	3.6	V
Input pin voltage, I/O	$V_{IO}$	-0.3	IOVDD+0.3	V
Input pin voltage, analog	$V_{ANA}$	-0.3	IOVDD+0.3	V

**Table 6. Absolute Maximum Ratings**

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

Item	Symbol	Min	Typical	Max	Unit
Operating temperature	$T_A$	-30		+85	°C
Supply voltage, analog , analog VDD_RF_IF and VDD_VCO	AVDD	2.7	3.0	3.3	V
Supply voltage, digital VDD_DIG	DVDD	2.7	3.0	3.3	V
Supply voltage, digital I/O VDD_IO	IOVDD	2.7	3.0	3.3	V

**Table 7. Recommended Operating Conditions**

AVDD and DVDD should be at the same voltage level; however, IOVDD may be at a different voltage level.

### Digital Signal Characteristics

Item	Symbol	Test Condition	Min	Max	Unit
Input high voltage	$V_{IH}$		0.7xIOVDD	IOVDD+0.3	V
Input low voltage	$V_{IL}$		-0.3	0.3xIOVDD	V
Output high voltage	$V_{OH}$	$I_{OH} = 1\text{mA}$	0.8xIOVDD	IOVDD	V
Output low voltage	$V_{OL}$	$I_{OL} = -1\text{mA}$	0	0.22xIOVDD	V
Input leakage current, at 25 °C	$I_{LI}$		-1.0	+1.0	μA

**Table 8. Digital DC Characteristics**

Item	Symbol	Min	Typical	Max	Unit
RF oscillator clock cycle	$t_{OSC}$		61 <sup>note 1</sup>		ns
RF oscillator setup time in clock cycles	$t_{STABIL}$		4096		Clocks
VCO setup time	$t_{vcostart}$			TBD	S
Clock cycle, CLKOUT	$t_C$		61 <sup>note 1</sup>		ns
Clock duty cycle, CLKOUT	$t_{DUTY}$	45		55	%
SPI Clock	$F_{SPI}$			5	MHz
Digital input pin capacitance	$C_i$			3	pF
Digital output load capacitance	$C_L$			20	pF

**Table 9. Digital AC Characteristics**

<sup>1</sup> Note that the RF oscillator frequency should be 16.3676 MHz for normal operation with the uN8031 baseband, so the 61 ns clock cycle is not exact.

### Typical Operating Power

The following are typical operating power estimates in different modes.

Item	Description	Conditions	Typical	Unit
Active Mode	State after XRES assertion with PWR_ON_OSC=1, all functions on with CTRL bits 3..0 set to 0	AVDD=3.0V DVDD=3.0V 25 °C	54	mW
Sleep, clock enabled	All functions disabled, PWR_ON_OSC=1 with CTRL bits 3..0 set to 1	AVDD=3.0V DVDD=3.0V 25 °C	3	mW
Sleep, clock disabled	All functions disabled, PWR_ON_OSC=0 with CTRL bits 3..0 set to 1	AVDD=3.0V DVDD=3.0V 25 °C	0.003	mW

**Table 10. Typical Operating Power**

### Analog Signal Characteristics

Item	Symbol	Min	Typical	Max	Unit
RF+/- input impedance	$Z_{RF}$		$x+yi$ <sup>note3</sup>		$\Omega$
XTAL IN input impedance	$Z_{XTI}$		1		M $\Omega$
I/Q gain imbalance	$G_{IQ}$			TBD	dB
Conversion gain <sup>note 4</sup>	G	70		106	dB
Phase noise <sup>note 5</sup>	NP			TBD	dBc
Noise figure	NF			15	dB
1 dB compression point at input	$P_{1dB}$		-20		dBm
Bandwidth	BW		4		MHz
XTAL IN input level	$V_{XTI}$	0.5	0.8	DVDD	V <sub>pp</sub>

**Table 11. Analog Signal Characteristics**

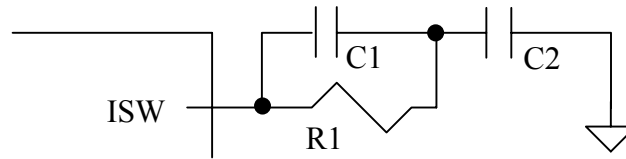
<sup>3</sup> The RF input impedance is complex and the given typical value is measured at 1575.42 MHz.

<sup>4</sup> The gain is adjustable with an adjustment range of 0 to 36 dB. The gain figures mentioned in the table correspond to situations where the gain has been set to its minimum and maximum values, respectively.

<sup>5</sup> Phase noise measurement is calculated as the difference in the signal level from the IF image reference point to a point 10KHz offset from the image.

**Applications Information**

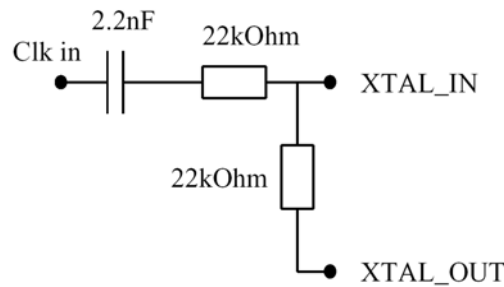
Though the loop filter can be implemented in a variety of ways, the recommended uN8021B VCO loop filter topology and component values are listed below:



**Figure 4. Recommend Loop Filter**

Item	Typical	Unit
R1	12K	ohm
C1	330	pF
C2	3.3	nF

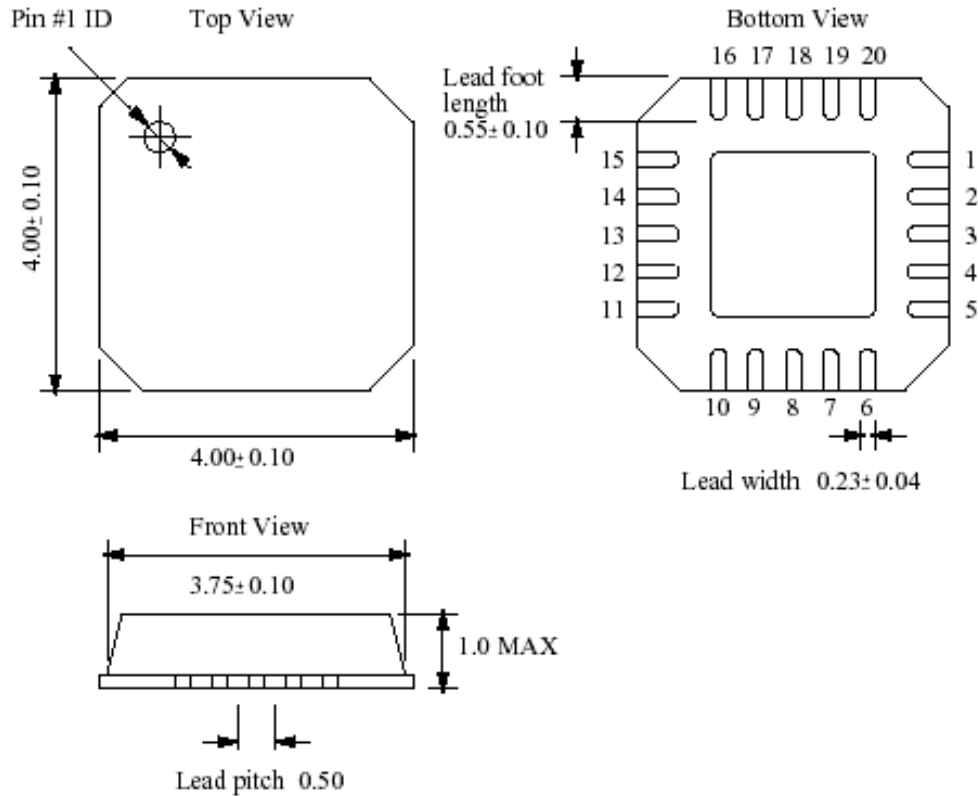
When using an external reference clock, the circuit below is recommended to attenuate and DC isolate the source. The voltage at XTAL\_IN must exceed minimum  $V_{XTI}$  volts.



**Figure 5. External Reference Clock Coupling**

### Package Description

The uN8021B is packaged into a QLP-20 package. The package dimensions (in millimeters) and pin numbers are as follows:



**Figure 4. uN8021B Package Outline**

Note that the pin numbers increase in the counterclockwise direction when viewed from above.

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