

# SST28SF040—4 Megabit SuperFlash EEPROM

## Command Interrupt Recovery



*Application Note*  
Revised March 1998

### 1.0 INTRODUCTION

The SST28SF040 SuperFlash EEPROM offers the ease of 5V-only reprogrammability along with the operational safety provided by the use of command registers. The command registers (non read) of the 12 volt flash EPROM devices require that 12 volts be present on  $V_{PP}$  for the registers to be active. The command registers of the SST28SF040 are active in the normal  $V_{CC}$  operating range. Inadvertent commands or command sequence interrupts could cause the SST28SF040 to be in a recoverable non-accessible state. The purpose of this application note is to provide a recognition method for this non-accessible state and a simple method to exit this state.

### 2.0 Device Operation

There are seven command operations used to initiate the memory operation functions of the device. They are 1) Sector-Erase, 2) Chip-Erase, 3) Byte-Program, 4) Reset, 5) Read-ID, 6) Software Data Protect, and 7) Software Data Unprotect.

The Software Data Protect and Unprotect command operations are read sequences. The device invokes these modes only upon the completion of seventh (last) byte. Any violation to the exact sequence of address cancels the mode and the SST28SF040 remains in the read mode.

The Read-ID command operation has only one command to enter the mode and therefore cannot be in a non-accessible state. However the device will remain in the Read-ID mode until a Reset command has been issued. No main memory operation can be performed while in the Read-ID mode. The Reset command operation reinitializes the command registers and returns the device to the Read mode.

The Sector-Erase, Chip-Erase, and Byte-Program command operations can put the SST28SF040 into a non-accessible state, if the command sequence is not properly carried out. These are two command operations, setup followed by execute, each with a specific sequence. An inadvertent command is defined as an erroneous command sequence (e.g., a setup command sent by the user for an operation not desired by the user, who wants to exit this operation without executing it).

### 2.1 Sector-Erase Operation

The Sector-Erase operation is initiated by a setup command and an execute command. The setup command stages the device for electrical erasing of all bytes within a sector (256 Bytes). The setup command is performed by writing (20H) to the device. To execute the Sector-Erase operation, the execute command (D0H) must be written to the device. The Erase operation begins with the rising edge of the WE# pulse and is terminated automatically by using an internal timer.

When the setup command is sent to the SST28SF040, the device's I/Os enter a high impedance state and will only accept data. This normally is not an issue since an execute command will follow and the device will perform a Sector-Erase. However if due to either a command sequence interrupt (e.g., a CPU interrupt) or an inadvertent command initiation, only the set-up command is sent, the SST28SF040 will remain in the high impedance (non-accessible) state and the device cannot be read.

### 2.2 Chip-Erase

The Chip-Erase operation is initiated by a setup command and an execute command. The setup command stages the device for electrical erasing of all bytes within the SST28SF040 (512 KBytes). The setup command is performed by writing (30H) to the device. To execute the Chip-Erase operation, the execute command (30H) must be written to the device. The Erase operation begins with the rising edge of the WE# pulse and is terminated automatically by using an internal timer.

When the setup command is sent to the SST28SF040, the device's I/Os enter a high impedance state and will only accept data. This normally is not an issue since an execute command will follow and the device will perform a Chip-Erase. However if due to either a command sequence interrupt (e.g., a CPU interrupt) or an inadvertent command initiation, only the set-up command is sent, the SST28SF040 will remain in the high impedance (non-accessible) state and the device cannot be read.



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## 2.3 Byte-Program Operation

The Byte-Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. The address bus is latched on the falling edge of WE#, CE#, or the rising edge of OE#, whichever occurs last. The data bus is latched on the rising edge of WE#, CE#, whichever occurs first. The programming operation begins with either the rising edge of WE#, CE#, whichever occurs first. The Program operation is terminated automatically by an internal timer.

When the setup command is sent to the SST28SF040, the device's I/Os enter a high impedance state and will only accept data. This normally is not an issue since an execute operation (WE# toggling) will follow and the device will perform a Byte-Program. However if due to either a command sequence interrupt (e.g., a CPU interrupt) or an inadvertent command initiation, only the set-up command is sent, the SST28SF040 will remain in the high impedance (non-accessible) state and the device cannot be read.

## 3.0 Non-Accessible State Detection

The SST28SF040 enters into a non-accessible state when the I/Os are at high impedance (e.g., will read as "FF"). The SST28SF040 will not read correctly in this state. When the application detects an unexpected "FF" state, reread the device twice more. If the device does not read correctly, then the device could be in the non-accessible state.

## 4.0 Reset Operation

A simple way to exit the SST28SF040 from the non-accessible state is to issue a Reset command. When the CPU interrupts either a Sector-Erase, a Chip-Erase, or a Byte-Program sequence, a Reset should be sent before beginning any operation on the SST28SF040. If a SST28SF040 should be in the non-accessible state (as described in the previous paragraph), a Reset should be issued.

The Reset command is provided as a means to safely abort the Erase or Program command sequences. Following any setup command (erase or program) with a write of (FFH) will safely abort the operation. Memory contents will not be altered. The Reset command returns the device to the read mode. The Reset command does not enable Software Data Protect.

## 5.0 Software Data Protection

Provisions have been made to further prevent inadvertent writes through software. In order to perform the write functions of Erase or Program, a two-step command sequence consisting of a setup command followed by an execute command avoids inadvertent erasing or programming of the device.

The SST28SF040 will default to Software Data Protect (SDP) after power-up. The SST28SF040 must be SDP disabled (Unprotect) in order to execute a write (erase or program) operation. SST strongly recommends the SST28SF040 have SDP enabled after the Write operation is completed. Software Data Protect is a global command and has specific sequences for enabling and disabling.

A sequence of seven consecutive reads at specified device addresses will disable SDP (unprotect the device). The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address has to be latched in the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will enable SDP (protect the device).

When the SST28SF040 is in the protected state a Sector-Erase, Chip-Erase, or Byte-Program operation will not alter memory. However the SST28SF040 will enter the high impedance state for a period of time equal to  $T_{RST}$  (4  $\mu$ s) after the execute command is sent. At the end of the 4 ms the SST28SF040 can be read.